Au-Ta$_2$O$_5$-SiO$_2$-Si capacitors were studied in order to investigate their dielectric characteristics and reliability. Tantalum pentoxide thin films on Si were prepared by two methods (RF sputtering of Ta in Ar + O$_2$ and thermal oxidation of tantalum layer on Si, with two thicknesses 50 nm and 17 nm). Films were subjected to post deposition oxygen annealing at 900$^\circ$C for 30 min. The leakage current density for d = 50 nm is under $10^{-7}$ A/cm$^2$ at 0.95–1 MV/cm for accumulation and at 0.5–0.64 MV/cm for inversion. For thinner structures (d = 17 nm) leakage current is much higher.

Investigation of the conduction mechanism confirms that SE dominates for low fields (till 4 V) and goes to Pool-Frenkel for medium fields (over 4 V) for accumulation regime and for reversed bias fast increase of the current is observed at 3–5 V which may be due to the breakdown of the ultrathin SiO$_2$ at the interface with Si. For this region the conduction mechanism may be combination of Fowler-Nordheim tunneling (FN) through SiO$_2$ and PF through Ta$_2$O$_5$.

Reliability tests show different dependences at the first stage for the structures with different thickness and different method of obtaining. Similar curves are observed for all currents injected. Breakdown field is over 2 MV/cm for thicker and ~ 6 MV/cm for thinner films. The structures show good characteristics for DRAM application, although high C-V and quasistatic C-V measurements show high degree of defects in the insulator layers.

**Key words:** Tantalum pentoxide, gold electrode, reliability, DRAM application.

1. **INTRODUCTION**

There is an extended demand for replacing poly silicon gates and silicon oxide with metal gates and alternative high-k gate dielectrics in MOS capacitors because of their thickness limitation. Scaling down the thickness of the film...
bellow 1 nm leads to tunneling effect, which increases rapidly the leakage current in the structure. In the last decade new materials with high dielectric constants such as Y$_2$O$_2$, ZrO$_3$, TiO$_2$ are intensively investigated. Most promising candidate for the next generation of integrated circuits instead of SiO$_2$ is Ta$_2$O$_5$ with its dielectric constant 25 [1, 2]. We spent last few years for investigating this material and its electrical and dielectric characteristics related to DRAM (dynamic random access memories) application [3–5].

Usually the material we used for gate was Al because of its deep application in the silicon industry. Investigating the conduction mechanism in these structures (Al-Ta$_2$O$_5$-Si) [4], we obtained for low fields applied possible Schottky emission (electrode limited emission), which led us to conclusion that we can make changes in the leakage currents by changing the work function between the metal gate and the poly-Si substrate. Next step was change of the gate material, i.e. Au with work function difference with semiconductor $\Phi_{\text{AuSi}} = 0.09$ eV, instead of Al with $\Phi_{\text{AlSi}} = 0.7$ eV, and further analyses of the leakage currents and conduction mechanism of such structures.

2. EXPERIMENT

Tantalum pentoxide thin films were deposited on p-type Si substrates (15 $\Omega$cm) by reactive sputtering of Ta-target in an Ar/O$_2$ mixture (O$_2$ content $N_c = 10\%$, substrate temperature $T_s = 473$ K) and thermal oxidation of tantalum layer on Si in dry oxygen at atmospheric pressure and oxidation temperature $T_{\text{ox}} = 873$ K (tantalum deposited on silicon by rf sputtering of Ta target in Ar atmosphere) [6]. The films were subsequently annealed in dry oxygen at 1123 K for 30 min. Thicknesses of the films measured by ellipsometry with laser light of $\lambda = 632.8$ nm are 50 nm for thermally oxidized films and 47 and 17 nm for rf sputtered ones.

MOS structures were formed with evaporation of 500 nm thick Au layer as a gate electrode. Four different areas were obtained for thicker films ($1 \times 10^{-4}$ cm$^2$, $2.25 \times 10^{-4}$ cm$^2$, $6.25 \times 10^{-4}$ cm$^2$ and $2.5 \times 10^{-3}$ cm$^2$) and area of $1.96 \times 10^{-3}$ cm$^2$ for thinner ones. According to the results of our previous measurements [7, 8] we suppose that the thin interlayer of SiO$_2$ is formed between Si substrate and the Ta$_2$O$_5$ insulator. This happens because of unavoidable oxidation of Si during the deposition procedure for both technological methods. The thickness of this layer is no bigger than 3 nm which influences to the total amount of the dielectric constant of the insulator layer.

$I$–$V$ characteristics for both gate polarities were measured using HP4140B picoammeter with step 0.1 V and rate 0.1 V/s with a delay time of 2.5 s. The same instrument was used for measuring quasistatic $C$–$V$ characteristics. High
frequency $C$–$V$ characteristics were measured with HP LCRmeter at 1 MHz with a step 10 mV. Reliability tests were made using HP 3458A multimeter, performing constant current stress measurements with injecting low currents from the gate (0.02 A/cm$^2$, 0.03 A/cm$^2$, 0.04 A/cm$^2$, 0.3 A/cm$^2$, 0.4 A/cm$^2$).

3. RESULTS AND DISCUSSION

The hysteresis effect was obtained for these structures. The $C$–$V$ curves were measured from –5 V to 5 V from accumulation to inversion and reverse. The shift for rf sputtered structures was –0.7 V and for thermally oxidized –0.4 V. This means a lot of imperfections which was shown during measuring of quasistatic characteristics. Because of a negative shift we believe that the capturing of the surface states at Si/SiO$_2$ interface takes place (Fig. 1). The value of accumulation capacity shows $C = 5.5 \text{ mF/cm}^2$ and $3.77 \text{ mF/cm}^2$ for thermally oxidized structures.

![Fig. 1. – Hysteresys effect for thermally oxidized structures.](image)

The leakage current density is found below $10^{-7}$ A/cm$^2$ till 4.5–5 V for accumulation and at 2.5–3 V for inversion for films with $d \sim 50$ nm. This corresponds to applied electrical field till 0.95–1 MV/cm for accumulation and 0.5–0.6 MV/cm for inversion, Fig. 2 and Fig. 3. The thinner films show much higher leakage current i.e. $0.5 \times 10^{-6}$ A/cm$^2$ for 5 V for accumulation and even higher for inversion.
The conduction mechanism was investigated for low fields in two terms: Pool-Frenkel mechanism, i.e. bulk limited which gives the dependence $\ln(J/E) \text{ vs } E^{1/2}$, where $J$ is current density, $E$ is applied electric field and Schottky emission i.e. electrode limited with dependence $\ln J \text{ vs } E^{1/2}$. The difference between these two conduction mechanisms is given in the exponent by factor 2. Also, in SE the current is expected to depend on the gate polarity while in PF it is not [9, 10]. It is obvious from the PF and SE dependencies given in Fig. 4 and Fig. 5 that there is a difference between the two polarities for medium fields (> 2.5 V). We can
also see that the linearity for SE indicates that conduction mechanism is SE. The obtained values for dielectric constant $K_T$ between 1.9–4.5 is very close to the optical dielectric constant with value 4.84 and confirms the SE.

Fig. 4. – $\ln J$ vs $E^{1/2}$ (Schottky emission).

Fig. 5. – $\ln (J/E)$ vs $E^{1/2}$ (Pool-Frenkel mechanism).
4. RELIABILITY TESTS

The structures were submitted to constant current stress injection from the gate. The comparison was made between the curves obtained for injected \( J = -0.02 \text{ A/cm}^2 \) for all three types of structures. Different behavior was observed for every single structure.

![Graph showing voltage dependence of time during constant current stress for all structures.](image)

During stress thicker rf structures show continuous degradation of the film; at first it is faster and later slower. The degradation of the first stage shows existing of negative traps at the interface Au/Ta_2O_5 which are filled with positive charge. At the second stage \( i.e. \) long times, where slow degradation of the structure is observed, we think that slow liberation of negative charge takes place \( i.e. \) neutral traps are freeing the electrons. The breakdown voltage was taken from the \( I–V \) curves where \( I \) overcomes the value of \( 10^{-4} \text{ A/cm}^2 \). It is estimated to 2.9 MV/cm (13.6 V).

The situation is different with thinner rf structures. At the beginning the voltage through the film increases, \( i.e. \) fast capturing of negative charge takes place, which means that positive traps catch electrons. The reason for this may be post metallization annealing in H_2 and the bigger presence of hydrogen in the interface. After the maximum voltage is approached the second stage starts (\( t > 50 \text{ s} \) ) and the behavior is similar with the behavior of the thicker films and
slow degradation starts. The curves on the figure show similar dependence for different injected currents for the same structures. The difference is observed in initial value of the voltage.

![Graph showing voltage dependence over time for different current densities.

Fig. 7. – Voltage dependence of time for different current density 0.01 A/cm² injected in the same structure rf sputtered with d = 17 nm.

We can mention here that for Ta₂O₅ structures one can rarely see catastrophic breakdown like in the SiO₂ structures; these films usually have slow degradation which is the reason for the prolonged breakdown. The value of the breakdown voltage is taken to be the higher value of the voltage which is around 9.5–10 V i.e. \( E \approx 5.6 \text{ MV/cm} \).

Thermally oxidized films show quite different behavior. For the whole time of injecting constant current through the structure the voltage grows slowly which indicates the slow capturing of negative charge. The breakdown voltage \( \sim 10 \text{ V i.e.}\) 2 MV/cm. We investigated the change of the leakage current for these films after short term constant current stress (Fig. 8). Small decrease of the current is observed after 3.6 mC/cm²; 7.2 mC/cm²; 14.4 mC/cm²; 21.6 mC/cm² and 28.8 mC/cm² injected through the gate. This confirms the conclusion that negative charge is increasing; lowering of the current shows decreasing of the positive charge.
5. CONCLUSIONS

RF sputtered Au-Ta$_2$O$_5$-SiO$_2$-Si structures show better characteristics for DRAM application. They have higher capacity density, higher breakdown voltage, lower leakage currents. With shrinking the thickness the leakage current grows, but the breakdown voltage is higher. Still a lot of work is to be done for improving the dielectric characteristics of Ta$_2$O$_5$ capacitors and involving such insulator in the industry of microelectronics.

REFERENCES