RICH Upgrade PDMDB PRR - Summary of Kintex-7 FPGA Testing in Radiation Environments, Extrapolations and Conclusions

F. MACIUC[1], L. COJOCARIU[1], V. PLACINTA[1]

[1] *Horia Hulubei National Institute for R&D in Physics and Nuclear Engineering (IFIN-HH)*

Abstract

The report summarizes the results from 3 tests in proton beam, 3 tests in ion beams, an X-ray testing and one mixed field testing. The latter involves a testing of a full PDMDB prototype and a realistic firmware. The cross-section for single event effects in CRAM, BRAM were measured together with logic failure rates and number of critical bits per firmware. When the FPGA is subject to about 10^{12} proton/cm^2, the CRAM error rates are constants for fixed temperature and correspond to a cross-section $\sigma_{SEU} \approx 0.5 \times 10^{-14} cm^2/bit$. The I/O ring oscillators implemented for 6 of the I/O banks in dedicated firmware showed I/O communication beak-downs and the dedicated SEM IP core and triplicated logic were also tested. The extrapolated error rates give as probable the equivalent loss of 100 MaPMT-channels in RICH for one hour in Phase-I.

1 Introduction

Kintex-7 is an SRAM device from Xilinx. The device considered for LHCb RICH Upgrade is XC7K70T-1FBG676C where XC7K70T represents the dice and FBG676C the packing. Given the large number of unused I/O pins, most radiation hardness tests were done on the smaller package FBG484C, with slightly smaller number of I/O pins and size, yet the same device XC7K70T was used. This does not affect the error rate measurements presented here, as not all input and outputs of the device are tested in the test-board version of the FPGA, whereas for CHARM test with the full PDMDB prototype, we used the XC7K70T-1FBG676C version, but we have not tested the input channels/pins and I/O Banks. In the following the package is assumed to be Copper free and preferably in naked dice version. The upper layer for this flipped chip is either made of about 60 micrometers thinned wafer, or, of unthinned wafer plus a thermal raisin of negligible thickness. This is essential for ion penetration, but is also done to decrease a potential target material in front of integrated circuit active layers on the bottom of the dice.

1.1 Kintex-7 FPGA, Resources, Technology and Firmware

The Kintex-7 device [1, 2], XC7K70T-1FBG676C, has: 6 I/O Banks, 4.86 Mb Block RAM (BRAM) in 36 kb blocks, about 18.88 Mb of configuration Memory (CRAM), a maximum of 300 user I/O (8 GTX transceivers with maximum data rates of 6.6Gb/s in FBG676, 185 HR high range 1.2-3.3 V I/O, 100 HP high-performance 1.2-1.8 V), 82000 flip-flops.

Kintex-7 and other chips in the same generation use TSMCs 28 nm CMOS technology platform with high performance and low power (HPL) process and high-k metal gate. Hafnium and Titan are the heaviest atoms used in the transistors.

The Kintex-7 Configuration memory is SRAM type, which makes it vulnerable to Single Event effects due to its technology and 28 nm scale. As declared by Xilinx, the Kintex-7 is not a radiation hardened device, not being classified Space-Grade or Military-Grade, hence we need to test the full range of scrubbing and error mitigation technique and be able to correct fast. Also the RICH team needs to able to interpret online and off-line the possible remaining errors which are left uncorrected by scrubbing and mitigation procedures.

Besides the LHCb-RICH PDMDB firmware tested for storage and output, the firmware used are optimized for the measurement of one or two type of errors in the FPGA resources. See the other talks in PRR session for description of the PDMDB firmware. The tests used the following firmwares each with multiple versions depending on the facility and dose rate:

1. Triple Modular Redundancy (TMR) Flip-Flop (FF) chain logic model implemented with Flip-Flop hardware - or registers SRL 32b and SRL 16b. Various TMR logic scheme were implemented with a voter for 3 FF chains, voter after each cell of triplicated FF, or mixed;
2. I/O ring oscillators designed in I/O Banks over multiple I/O associated Blocks, e.g. basic I/O logic blocks. Each ring oscillator tests simultaneously the I/O logic of an I/O chains of blocks, the connectivity and the I/O:
3. BRAM read and write firmware, which allows to monitor online during the irradiation of the FPGA the changes in BRAM configuration and save results for data analysis.
4. LHCb-RICH PDMDB firmware using a static buffer and with an output of the stored

pattern through an optic cable at a rate of 40 MHz per pattern.

1.1.1 SEM IP Core Tool

LogiCORE IP controller [3] or Soft Error Mitigation (SEM) IP core allows Kintex-7 - and in general the 7th generation chips from Xilinx - to perform checks in configuration memory, to identify upsets with CRAM corruption, classify the memory corruption (single event upset classification), and a lot of times is able to correct the CRAM. The user logic can enable the SEM IP Core and use this tool to count the errors in CRAM, classify and correct. A testing firmware which uses the SEM IP core is able to provide to the user the error rates for each class. Assuming very high dose rate and High Energy Hadron (HEH) fluence, we have used the SEM IP Core in conjunction with a blind scrubbing procedure, which allows us to count and correct the CRAM errors online during irradiation and to reprogram the firmware into the device each time the SEM IP Core becomes idle or its logic is corrupted by radiation. We also have the information stored for off-line analysis.

1.2 Memory, JTAG, Essential Bits, Critical bits and User Logic

The sum of Kintex-7 memory includes CRAM, BRAM, distributed, FF, and a very small reserved registers and state bits. Except for the PDMDB test, the device is running run in JTAG mode, without any external flash configuration memory, which is close to the LHCb-RICH configuration.

The total CRAM memory of almost 20 Mb includes a much smaller number of essential bits, used by firmware to configure the user logic into device. The typical number of essential bits is 300 kb to 500 kb for our type of applications. From these essential bits only a fraction is critical to the user logic. In case these critical bits are corrupted, the transmitted information can be lost or scrambled. The logic failure depends on what the user defines as critical in the implemented logic, hence the number of critical bits can vary extremely from a few kilo-bits to the full number of the essential bits. The definition of essential bits is done by device producer, Xilinx, and depends on the logic and allocated resources.

We hence forward define the logic failure depending on the correct transmission of a given pattern, and we impose a condition with close to 100 % success rate. The transient bit flip in pattern and the permanent corruption of the pattern (could also have an intermittent behavior) are considered separately. The BRAM read/write firmware is distinct in the sense the pattern is fixed on the BRAM, and the reading is considered 100 % reliable in the special runs which test this logic - this is allowed because the constraints imposed in the beam flux and fluence for these dedicated runs.

1.3 Single Event Effects and Cumulative Effects

During this report we measure single event effects (SEE) caused by radiation in Kintex-7 resources. The single event effects can be software and hardware. Among the software effects are the Single Event Upsets (SEU) assumed permanent till next scrubbing or reprograming of device and the single-event transient (SET). The latter is a change in a local voltage on device which could propagate in the transmission and flip a single or

multiple bits. Compared with the SEU in memory which represent a change in state the SET effect is limited in time to values under clock precision. Only the latch in the bit pattern over a cycle or in the CRAM makes this effect visible during our tests. In case the SET is latched in the device memory like CRAM, then the SET becomes a SEU. Most probable, the large majority of CRAM errors - or CRAM SEUs - observed during the runs described below are of this nature.

The cumulative effects can affect a FPGA and in general an integrated circuit at hardware level, e.g. by inducing leakage currents in transistors or creating alternative pathways through parasitic transistors. The two classes of cumulative effects are total ionization dose (TID) effects and displacement damage (DD) effects. The former is visible in our ionizing radiation tests like proton-beam and X-ray irradiation, whereas the displacement damage is investigated in proton-beam runs. The ion-beam runs are dedicated exclusively to SEE detection.

1.4 Proton, Ion, Mixed-Field and X-ray Facilities

The proton-beam runs were done at: Proton Irradiation Facility (PIF) in Paul Scherrer Institut; and at Institut für Kernphysik (IKP) within Juelich Forschungzentrum. We have used protons with 200 MeV delivered by COMET cyclotron at PSI and the 35 MeV proton beam from JULIC cyclotron, over several runs. Each run had typical fluence of up to 10^{12} protons per cm^2. The cumulative TID was between 200 and 600 krad (6 Gy) per each tested device at PSI and between 200 krad and 1 Mrad (1 kGy) at Juelich for each FPGA. An average value of dose rate is 10 krad/s and 10^8 cm^{-2} per high TID and fluence runs. The low flux runs had 10^6 cm^{-2} for BRAM runs.

The SIlicon and RADiation (SIRAD) [4] facility is using the Legnaro National Laboratory (LNL) 15 MV TANDEM accelerator to accelerate ions and protons. We have so far used Florine, Oxygen and Silicon ions with 3.7 to 13.4 MeV cm^2 /mg linear energy transfer (LET) or stopping power. In Louvain the Heavy Ion Irradiation Facility (HIF) uses the CYCLONE beam from CRC to accelerate ions from Carbon to Xenon. We have used Carbon, Neon, Argon, Nickel and Krypton ions with LET from 1.3 MeV cm^2 /mg to 32 MeV cm^2 /mg.

The mixed field radiation facility at CERN, CHARM, uses PS proton on various type of targets to produced a mixed environment with mostly high energy neutrons (>20 MeV). We have used 4 PDMDB prototype boards, monitored online over 50 m cable, operating in realistic conditions. The TID is 34 krad (340 Gy) and 1.06$\times$ 10^{12} cm^{-2} for position 10 in CHARM irradiation room, which correspond close to the LHC tunnel conditions.

The X-ray facility in Padova University - Seifert RP-149 Semiconductor Irradiation System - has Tungsten anode with continuous spectrum from 8 to 60 keV and L lines from 8 to 12 keV. The total TID on the tested boards was 200 krads and 300 krads.

1.5 LHCb RICH1 and RICH2 environments for Phase-I

The radiation in Phase-I was estimated by LHCb dedicated group based on Fluka simulations with LHCb geometry. The results in 1 include the LHCb results presented during one of LHCb Collaboration Week meeting.

The radiation environment has the TID dominated by a large gamma and lepton (electromagnetic) contribution plus slow neutron component.The HEH contribution to

Table 1: LHCb RICH1 and RICH2 environments, worst (best) case scenario for HEH, TID and 1-MeV neutron equivalent

	HEH (E>20 MeV) (cm^{-2})	Dose (Gy)	1-MeV neq (cm^{-2})
RICH 1	1.2×10^{12} (0.5×10^{12})	200 (31)	3.1×10^{12} (1.9×10^{12})
RICH 2	0.5×10^{12} (0.29×10^{12})	80 (23)	1.6×10^{12} (0.9×10^{12})

TID is smaller, yet it is this component which generates SEE in Kintex-7.

2 Test Bench of Kintex-7, Test Parameters, Monitoring and Measurements

The test bench for the Kintex-7 FPGA includes a dedicate PCB made by our group, which allows programming of device through JTAG interface. The power is supplied to 1.8 , 1, 1.5 (no current in 1.5 V I/O in initial configuration), 3.3 V power rails. Unlike PDMDB communication, the pattern communication for this test PCB is serial (close to UART).

2.1 DAQ system

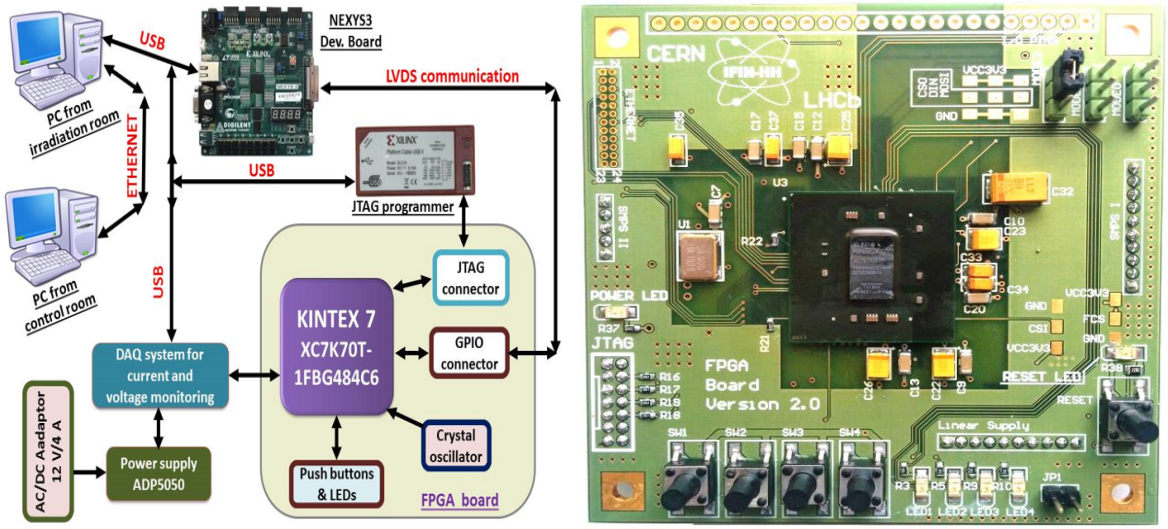
A detailed description of the DAQ is given in [5] and Vlad's talks and proceeding ([6] at TWEPP conferences in 2016 and 2017. We summarize here few key aspects regarding the monitored parameters. We store the measured currents and voltages on 1.8, 1 and 3.3 rails each 25 ms for latter analysis of SEL and SEU effects. The Single Event Latch-ups are measured as sudden jumps in currents and a small fraction of SEUs generate the same structure except that the reprogramming or the SEM IP Core scrubbing remove the Upset and bring down the voltage. The schematics of the test-bench is displayed in the Fig. 1 together with the layout of the test board.

In PDMDB tests, the currents and voltages are read over DC-DC units, and a separate description is included at the of this chapter. The PDMDB communication and control is done over miniDAQ unit like in real conditions. Except the inputs which were not tested, the FPGA stored pattern is read over the FPGA to GBTx connection and into miniDAQ [1].

2.2 GUI

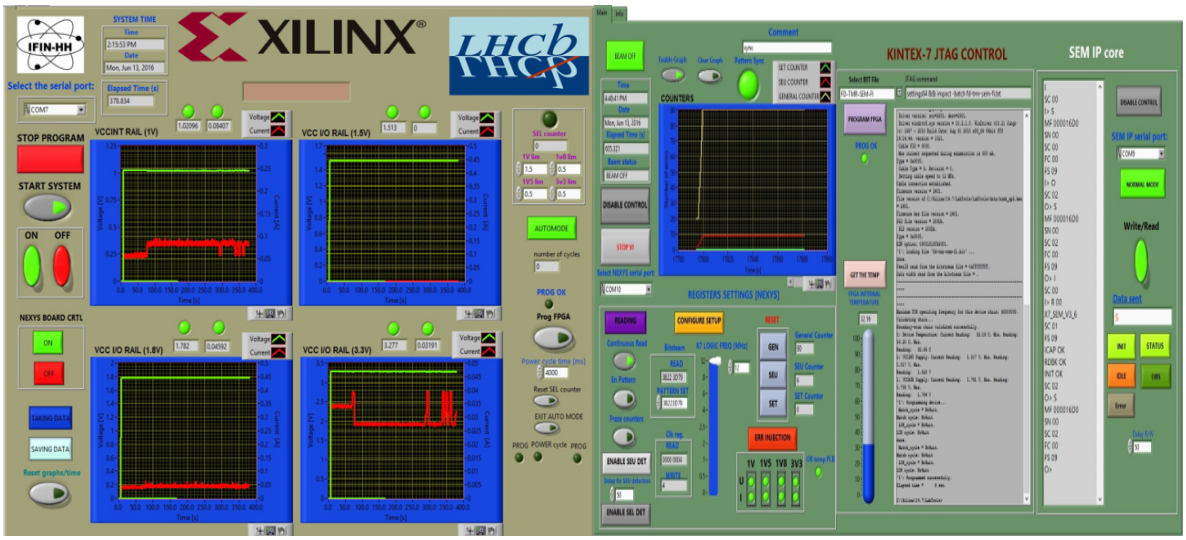
The Graphic User Interface controls the reprogramming, stores the voltages and currents, allows the online monitoring, saves the changes in the transmitted pattern, and controls the scrubbing. It is implemented in LabVIEW, and incorporates graphic display of the stored voltages and currents, in case of CHARM tests were 4 PDMDB were used we designed a GUI with a display of 32 power-related parameters, an online SEM IP core report, GUI control of scrubbing, automatic power-on and power-off procedures (e.g. blind scrubbing with power cycle) for high dose rate tests, etc. The Kintex-7 test-board GUI is given in Fig. 2.

[1] https://twiki.cern.ch/twiki/bin/view/LHCb/RichTestBeamMiniDaq



(a) (b)

Figure 1: (a) DAQ system in configuration for for test board; (b) test board with FPGA.



(a) (b)

Figure 2: (a) Current and voltage online display for 1, 1.8, 1.5, 3.3 V rails; (b) GUI for pattern check (logic failures) and SEM IP core report - all parameters are saved for off-line analysis, at each 0.2 seconds;

After calibrating the dose-rate and flux to match the capabilities of the measurement system and the failure rate of SEM IP core we count the SEU rate and do a fist estimation of cross-section per device given a certain fluency.

The SEM IP Core - in enhanced repair or simple repair mode - counts the number of

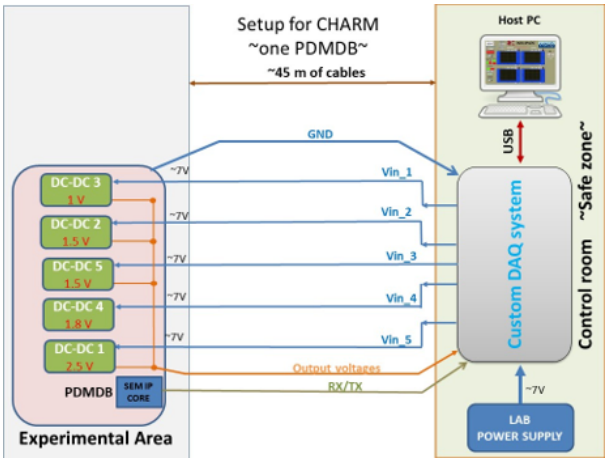


Figure 3: CHARM DAQ powers-on the 4 PDMDBDs and monitors the currents and voltages, controls and saves the output of SEM IP Core, the PDMDB to miniDAQ links are a independent and the GUI receives the information of logical errors from miniDAQ and counts them.

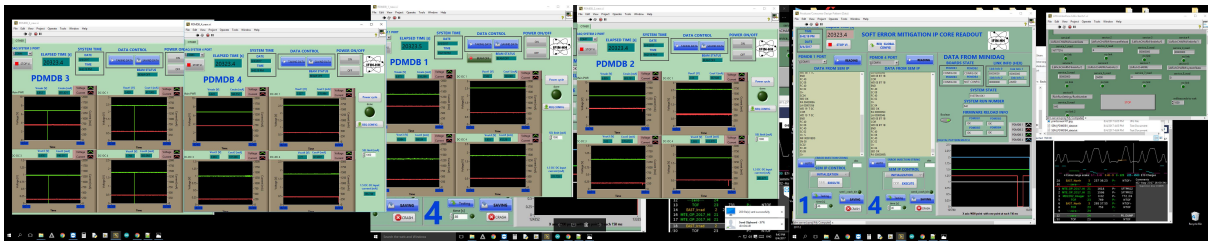


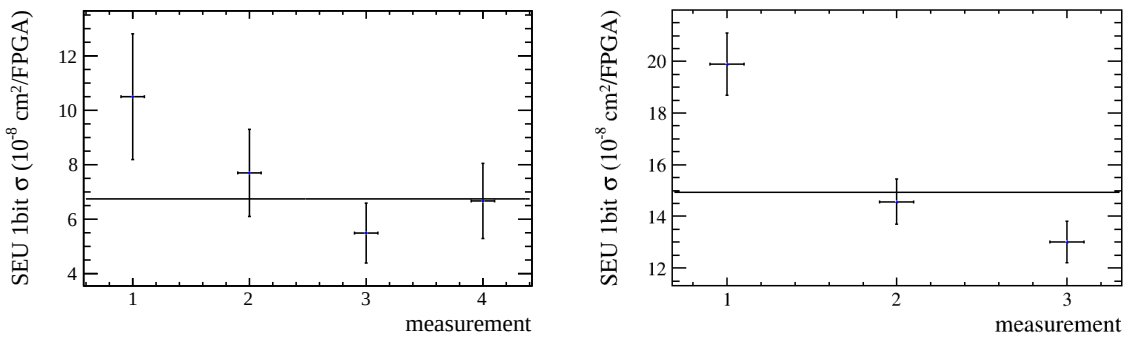
Figure 4: screen-shot during measurements, 4 PDMDB, 32 monitoring parameters, beam status, pattern agreement, SEM IP core interface over 2 PDMDB.

Upsets in configuration.

2.3 CHARM test DAQ

In CHARM tests the DAQ used the full PDMDB prototype with the DAQ and power supply connected directly to the DC-DC units on the PDMDB (Fig. **??**) and a fixed pattern read over the optic link from the 4 PDMDBs in CHARM facility to the miniDAQ in the control room. Any disagreement in the received pattern was communicated to the first DAQ dedicated DAQ system and logged into LabVIEW GUI, Fig 4.

For the last week of data taking in CHARM, we had available also the number of bits modified in the pattern, and on average over all observed Upsets in logic shows a value closer to 3 bits modified per pattern sequence.



(a) (b)

Figure 5: (a) PSI measurements in few of these runs with fit to $\sigma_{SEU} = 6.8 \pm 0.8$ cm^2 (fluence dominated error); (b) JULIC data at Juelich with CRAM cross-section of $\sigma_{SEU} = 15.0 \pm 1.8$ cm^2

3 Test Results

3.1 SEU and SEL Rates in Ion-beam Testing

Most ion results were already given in the EDR of PDMDB in 2016 [2]. We shall just summarize some of the most critical point in the following paragraphs and outline the results obtained for a few runs taken in 2017. The tests were made in Louvain at CRC at Heavy Ion Facility and at LNL in SIRAD facility.

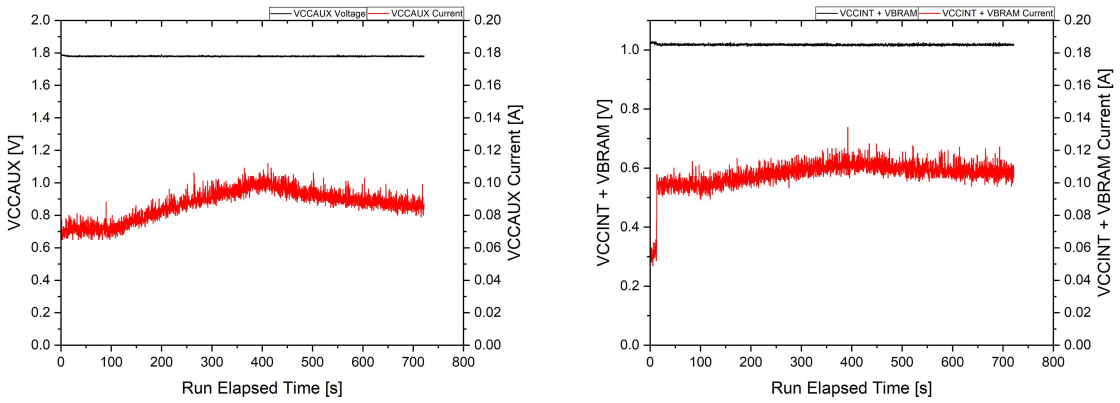
The HIF data showed that the SEU rate is significant above 1.3 MeV cm^2/mg pointing to a threshold around 1 MeV cm^2/mg. The plateau in obtained for a LET between 10 and 20 MeV cm^2/mg. At around 15 MeV cm^2/mg we have the threshold for the "micro"-latch-ups, SEL with discrete jumps in current on 1.8 V rail of 70 to 100 mA.

The BRAM SEU and Flip-Flop SEU in ion run are harder to measure due to CRAM corruption during data taking and can not be with 100 % confidence separated from CRAM SEU effects. We just conclude for ion runs that the BRAM and FF SEU have error rates of same order of magnitude with CRAM SEU. The I/O ring oscillators in the single Silicon ion test at LNL give 3 SEUs and 8 possible SETs for a fluence of 5×10^5 Si ions cm^{-2}. The SEU set is here most certainly due to CRAM corruption which modifies either the I/O block configuration or the ring oscillator routing. The observed transient effects are events without CRAM corruption, possibly in I/O block hardware.

3.2 Proton-beam Testing and SEU Cross-Sections

For CRAM testing in proton beam runs, we have used the PSI COMET (PIF) and JULIC cyclotrons with 200 MeV and 35 MeV protons, respectively. The results show good agreement with the expected values extrapolated from measurements in literature with CRAM SEU cross-section close to 10^{-7} cm^2. and no Latch-up events for these sub-GeV energies.

[2] https://indico.cern.ch/event/515232/attachments/1287757/1937933/PDMDB-EDR-Radiation-Hardware.pdf



(a) (b)

Figure 6: (a) TID effect after 100 krads, and for a Dose rate of 160 krads, the current increases on the 1.8 V rail ; (b) TID effect in STI after 100 krads, and for Dose rate of 160 krads, the current increases on the core (1 V rail).

The BRAM cross-section was estimated from low fluence and flux runs at JULIC in Juelich : 6.9×10^{-15} cm^2/bit. It is very close to 8×10^{-15} cm^2/bit for CRAM. This also validates the preliminary results in ion runs for the BRAM. The Flip-Flop Upsets are still impossible to distinguish from CRAM corruption, yet the assumption that the two cross-section are close seem to hold.

Four ring oscillators were implemented close to 70% I/O blocks located in 5 banks out of the 6 I/O banks of the device. The cross-section lower bound for SEU in these 5 ring oscillators is:

$$\sigma_{I/O} > 3 \times 10^{-11}\text{cm}^2,$$

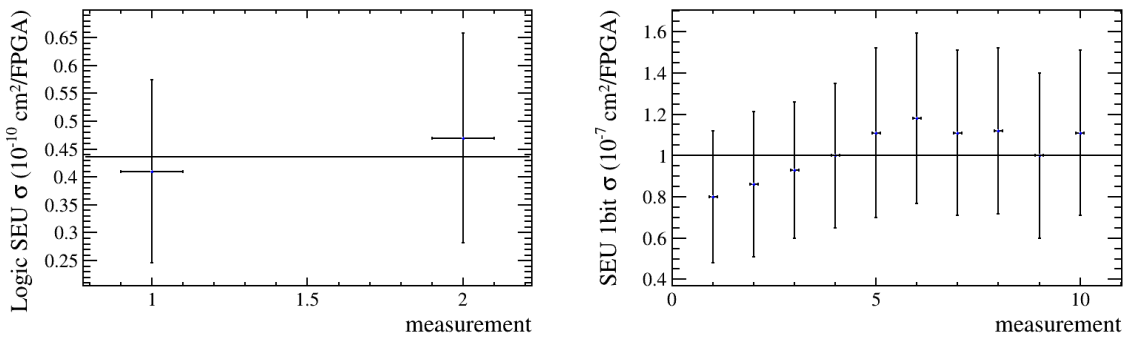
which in turn gives more then 90 events over Phase I for one PDMDB with 3 FPGAs. The scale factors regarding the I/O corrections and possible complications due to modified HEH spectra above 1GeV will be discussed in the end of this report.

Various versions of TMR were tested but due to nature of SRAM configuration memory and the SET latch in CRAM, we do not expect the TMR to be very efficient in prevention of errors and we gain only an estimated factor of 2 at most for a simple TMR and comparable for the rest of the TMR choices.

3.3 X-ray Testing and TID

As expected, a test on 2 devices showed no visible SEE in case of X-ray irradiation of Kintex-7, however there is clear indication TID effect after 100 krad, see Fig 7. The dose rate was 160-170 rads/s in runs of about 50 krads with 5-10 minutes in between.

The total TID for first board, was 160 krads and 150 krads for the second board. The annealing is clear in figure 7.



(a) (b)

Figure 7: (a) Logic failure cross-section in each of 2 weeks at CHARM averaged over 2 distinct PDMDBs in first week and 3 PDMDBs in last week ; (b) Total SEU cross-section in CHARM for one PDMDB;

3.4 CHARM Test of PDMDB Prototypes

The main test on Kintex-7 was done at CHARM in 2017. Our group and the UK groups have irradiated 4 PDMDB prototypes in CHARM, with the results already communicated to collaboration. We have measured here the CRAM SEU rate (through SEM IP core), the changes in current and voltage over 3 DC-DC out of 5 - only one FPGA and one GBTx were on the board, and this gives less power requirements. The main measurements were: the number of logic errors for the static pattern read over the GBTx and the GBT-SCA communication between miniDAQ and PDMDB.

During the CHARM test only the storage of a pattern and the read-out were tested, without imposing any criterion on input channels. Hence here a factor should be considered.

The cross-section for logic failures in one FPGA has the average over each week $\sigma_1 = 0,41 \times 10^{-10} cm^2$ (40% error, dominated by fluency uncertainty) and $\sigma_2 = 0,47 \times 10^{-10} cm^2$ (40 % error, dominated by fluency uncertainty). The total SEU rate has the corrresponding cross-section 10^{-7} cm^2 per FPGA and 5.4×10^{-15} cm^2 per bit for 18.8 Mb CRAM.

The number of critical bits in PDMDB firmware in Kintex-7 is the ratios of cross-sections times the total CRAM, hence about 8 kb out of 18.8 Mb CRAM. We take into account in the next section a multiplicative factor to account for untested write part of the final firmware.

4 Extrapolation, Conclusions

4.1 Extrapolation of Tests Results in LHCb Environment for Phase I

The numbers that were obtained during tests, especially those of CHARM tests, are propagated to LHCb-RICH case.

In the extrapolation to Phase I of the test results, we use the 7000 hours duration as approximation for the Phase I and for RICH 1 and RICH 2 we take the maximum

expected TID of 200 krads and 80 krads and corresponding fluences, respectively. The number of PDMDB FPGAs operating in Phase I for RICH1 is taken as 720, where as for RICH2 we consider 288 (FPGAs) for the Elementary Cells with 1 inch MaPMT and 192 FPGAs for the cells with 2 inch tubes. In total we have 1200 FPGAs, 720 (RICH1) and 480 RICH2.

Given an overall Phase-I fluence is 1.2×10^{12} HEH cm^{-2} in RICH1, and 0.5×10^{12} cm^{-2} in RICH2, we use a cross-section of SEU of 2×10^{-7} cm^2, with a safety factor of 2 to account for the difference in LHC tunnel radiation environment and the LHCb-RICH environment in Phase I, RICH being closer to an interaction point.

$$\frac{\Delta N_{SEU}}{\Delta t} = \left(2.4 \times 10^5 \times 720 + 10^5 \times 480\right) / 7000h \approx 32000/h \qquad \text{average over one hour}$$

Most SEU errors do not affect the firmware logic, but a very small fraction might induce current changes in FPGA for I/O banks and core. This changes are much like SELs, but unlike SEL they are removed by reprogramming or scrubbing.

CHARM and proton data did not include SELs, yet the PDMDBs need to be prepare for the eventuality of hardware changes like micro-Latch-ups.

The I/O error number per FPGA was found to be 30 over Phase I. We need to include again the multiplicative factors for uncertainty in SEU number and for the harder HEH spectrum in LHCb. The

$$\frac{\Delta N_{I/O}}{\Delta t} = \left(30 \times 720 + 15 \times 480\right) / 7000h = 4 \qquad \text{I/O SEU average over one hour;}$$

The upper number would be associated on the average to 3 channels.

When computing the number of logic failures we need to take into account besides the fluence, the SEU cross-section and the fraction of critical bits in the FPGA firmware. The should be at least a factor of 2 for the uncertainty in the number of critical bits and an other multiplicative factor for the HEH-spectrum harness in RICH compared to LHC-tunnel.

$$\frac{\Delta N_{Logic}}{\Delta t} = \left(4 \times 50 \times 720 + 4 \times 25 \times 480\right) / 7000h = 28 \qquad \text{Logic failures over one hour;}$$

Again, upper number should be associated on the average to SEU failures over 3 channels. During a long run of 8 hours we could get a number of 800 channel failures (1% of total), hence an error mitigation during run time should be implemented, and not left for off-line.

The TID effect should not be visible in phase I, as the dose rate is 3 order of magnitude lower than the test dose rate for which this effect was seen.

At level of MaPMT channels we could loose about 100 channels in one hour. Based on the available information to date, we consider this value to be the most probable order of magnitude for Phase I. The main uncertainty in this number represents the number of critical bits in firmware and the extrapolation error from CHARM environment to LHCb-RICH. One other source of uncertainty is the I/O block failure rate evolution in time and the effects on other devices.

4.2 Conclusions

Though not optimal from point of view of radiation hardness, the Kintex-7 FPGA is so far adequate for its task within PDMDBD of RICH in Phase I. The error rate per hour does seem to be manageable, and we hope we have foreseen the most important sources of uncertainties and accounted for them.

The LHCb-RICH collaboration has a backup solution for Kintex-7 in case the SEU and SEL rate will prove to be unmanageable in Phase-I for Kintex-7.

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